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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/557,520	01/30/2007	Minoru Ishikawa	00684.522762.	8818

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EXAMINER

MOORAD, WASEEM

ART UNIT	PAPER NUMBER
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2629

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/557,520	Applicant(s) ISHIKAWA ET AL.	
	Examiner WASEEM MOORAD	Art Unit 2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 March 2009.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5,8 and 9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5,8 and 9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 November 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/10/09 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oda (US 5,646,377) in view of Yoshida et al. (US 5,798,756).

Regarding Claim 1, Oda teaches a coordinate input apparatus, comprising:

A panel provided with a plurality of X interconnecting lines and a plurality of Y interconnecting lines disposed to intersect with each other in a matrix fashion (Figure 1)

Closed loop forming circuits disposed at two opposite ends of the display panel (Figures 1, 14, and 19, where Figure 1 and 19 show the opposite ends of the display panel and Figure 14 shows the closed loop forming circuits),

Switching circuits connected to a terminal of each of the X and Y interconnecting lines (Figure 14; column 17, lines 1-15; Figure 1, elements 22/23);

A detection circuit for detecting signals outputted from the closed loop forming circuits in the coordinate detection drive mode in response to a position indicator for indicating a position in a coordinate input area of the panel where the X interconnecting lines and the Y interconnecting lines are disposed in the matrix fashion (Figure 1, element 50, column 17, lines 1-40);

Wherein, in the coordinate detection drive mode, the closed loop forming circuits disposed at two ends of the display panel connect at least a pair of the terminals of the X interconnecting lines in each end to form a multiple closed loop of the X interconnecting lines and connect at least a pair of terminals of the Y interconnecting lines at each end to form a multiple closed loop of the Y interconnecting lines (Figure 14, column 17, lines 1-15).

Oda does not teach a display panel provided with a plurality of X and Y interconnecting lines disposed to intersect with each other in a matrix fashion, display drive circuits for supplying drive signals to the X and Y interconnecting lines in a display drive mode, closed loop forming circuits disposed at another two opposite ends of the display panel, and switching circuits connecting the X or Y interconnecting lines to the

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display drive circuits in the display drive mode and to the closed loop forming circuits in a coordinate detection drive mode.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Oda such that the closed loop forming circuits were also disposed at another two opposite ends of the display panel as an alternative design choice such that the X interconnecting lines could be connected with a pair of closed loop forming circuits and the Y interconnecting lines could be connected with another pair of closed loop forming circuits.

Yoshida et al. teaches the coordinate input area is formed in a display panel (column 7, lines 16-30; where the panel is an LCD panel) and further teaches a circuit for switching a display drive mode using the matrix of the X and Y interconnecting lines and a coordinate detection drive mode using the matrix of the X and Y interconnecting lines (Figure 1, element 108; column 18, lines 19-25; where the changeover control circuit switches between the display driving circuit and the coordinate detection circuit).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Oda with the teachings of Yoshida et al. by having the coordinate input area formed in a display panel with a switching circuit between a display drive mode and coordinate detection mode, as well as the closed loop circuit operating the coordinate detection drive mode so the user can be given the option of looking at the display in the display drive mode or using the coordinate detection mode in order to determine the coordinates of a display panel (column 7, lines 32-36).

Regarding Claim 2, Oda teaches wherein the closed loop includes a switch circuit for selecting first to four X interconnecting lines from the plurality of interconnecting lines so that: a first terminal of the first interconnecting line is connected with a first terminal of the second interconnecting line, a first terminal of the third interconnecting line is connected with a first output terminal, a second terminal of the third interconnecting line is connected with a second terminal of the first interconnecting line, a first terminal of the fourth interconnecting line is connected with a second output terminal, and a second terminal of the fourth interconnecting line is connected with a second terminal of the second interconnecting line (Figure 14c, where a double closed-loop circuit comprises a switch circuit from selecting a plurality of interconnecting lines and connects them accordingly. The first line is the 4th terminal, the second line is the 1st terminal, the third line is the 2nd terminal, and the fourth line is the 3rd terminal).

Regarding Claim 3, Oda teaches wherein the closed loop includes a switch circuit for selecting first to four Y interconnecting lines from the plurality of interconnecting lines so that: a first terminal of the first interconnecting line is connected with a first terminal of the second interconnecting line, a first terminal of the third interconnecting line is connected with a first output terminal, a second terminal of the third interconnecting line is connected with a second terminal of the first interconnecting line, a first terminal of the fourth interconnecting line is connected with a second output terminal, and a second terminal of the fourth interconnecting line is connected with a

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second terminal of the second interconnecting line (Figure 14c, where a double closed-loop circuit comprises a switch circuit from selecting a plurality of interconnecting lines and connects them accordingly. The first line is the 4th terminal, the second line is the 1st terminal, the third line is the 2nd terminal, and the fourth line is the 3rd terminal).

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oda (US 5,646,377) in view of Yoshida et al. (US 5,798,756) and further in view of Morita (US 5,128,499)

Regarding Claim 4, it is analyzed with respect to the analysis of Claim 1. Oda., in view of Yoshida et al., is silent regarding wherein the closed loop is sequentially formed at a constant pitch on the matrix of the X and Y interconnecting lines with a lapse of time.

Morita teaches wherein the closed loop is sequentially formed at a constant pitch on the matrix of the X and Y interconnecting lines with a lapse of time (Figure 1, column 3, lines 65-68; where the closed loop has a constant pitch, element Ps)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Oda, in view of Yoshida et al., with the teachings of Morita by having a closed loop formed at a constant pitch so to have equal conductivity between each of the sense lines on the X-Y matrix.

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5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oda (US 5,646,377) in view of Yoshida et al. (US 5,798,756) and further in view of Watanbe et al. (US 5,567,920).

Regarding Claim 5, it is analyzed with respect to the analysis of Claim 1. Oda in view of Yoshida et al., is silent regarding wherein on the matrix of the X and Y interconnecting lines, a closed loop formed timewise previously and a subsequent closed loop formed after the closed loop are selected to have an embedded structure.

Watanbe et al. teaches wherein on the matrix of the X and Y interconnecting lines, a closed loop formed timewise previously and a subsequent closed loop formed after the closed loop are selected to have an embedded structure (Figure 18, column 20, lines 22-32; where an embedded structure is formed with the closed loop and the subsequent closed loop)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Oda., in view of Yoshida et al., with the teachings of Watanbe et al. by having a closed loop and a subsequent closed loop to have an embedded structure so that electromagnetic coupling is cancelled (column 20, lines 28-32).

6. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oda (US 5,646,377) in view of Yoshida et al. (US 5,798,756) and further in view of Kawai (US 2003/0086149)

Regarding Claim 8, it is analyzed with respect to Claim 1. Oda., in view of Yoshida et al., does not teach the display panel having a memory characteristic.

Kawai teaches an electrophoretic display having a memory characteristic (page 1, section 0003).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Oda, in view of Yoshida et al. with the teachings of Kawai by having a display panel having a memory characteristic so to have the ability to hold a display image (page 1, section 0003)

Regarding Claim 9, it is analyzed with respect to the analysis of Claim 8. Kawai further teaches the display panel being an electrophoretic display panel (page 1, section 0003).

Response to Arguments

4. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argues that the Sudo reference does not teach "closed loop forming circuits disposed at two opposite ends of the display panel and at another two opposite ends of the display panel"

Examiner fully considers and agrees with Applicant's arguments, however, the arguments are moot in view of the new grounds of rejection in view of Oda ('377)

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Oda ('377) teaches closed loop forming circuits disposed at two opposite ends of the display panel (Figure 1, Figure 19, elements 22/23 where the loop coil switching units possess closed loop forming circuits, demonstrated in Figure 14, which are connected to X and Y lines as stated in column 17, lines 1-5). Oda ('377) does not teach another pair of closed loop forming circuits disposed at another two opposite ends of the display panel. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings to Oda such that rather than 2 ends having closed forming circuits, there will now be 4 closed loop forming circuits disposed all around the display panel such that it is alternative design choice providing a pair for X interconnecting lines and another pair for Y interconnecting lines.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to WASEEM MOORAD whose telephone number is (571)270-3436. The examiner can normally be reached on M-F 730am-4pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on 571-272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Waseem Moorad/
Examiner, Art Unit 2629

/Amr Awad/
Supervisory Patent Examiner, Art Unit 2629

05/19/09